
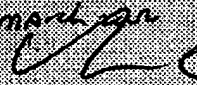


PATENT
Docket No. 2885/16

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor  VORBACH et al.
Serial No. 09/145,139
Filing Date August 28, 1998
For: **INTERNAL BUS SYSTEM FOR DFPS AND UNITS
WITH TWO-OR MULTI-DIMENSIONAL
PROGRAMMABLE CELL ARCHITECTURES, FOR
MANAGING LARGE VOLUMES OF DATA WITH A
HIGH INTERCONNECTION COMPLEXITY**
Examiner : VO, Tim T.
Art Unit : 2181

Assistant Commissioner
for Patents
Washington D.C. 20231
Box ISSUE FEE

I hereby certify that this correspondence is being deposited with the
United States Postal Service as first class mail in an envelope addressed
to: Assistant Commissioner for Patents, Washington, D.C. 20231 on
Date: 29 March 2002 Reg. No. 36,098
Signature: 
Michelle M. Carman

AMENDMENT UNDER 37 C.F.R. § 1.312

A notice of allowability issued for the above-identified application on
December 31, 2001. The issue fee is being paid concurrently herewith. Please amend the
application under 37 C.F.R. § 1.312 as follows:

IN THE SPECIFICATION:

✓
Please replace the paragraph beginning at page 3, line 31 with the following rewritten
paragraph:

E1 -- Figures 15a-15d and 15f-15h show the status of a data transfer of a connection
release at intervals of one bus cycle. --